

Towards a novel silicon timing detector: ATLAS HGTD

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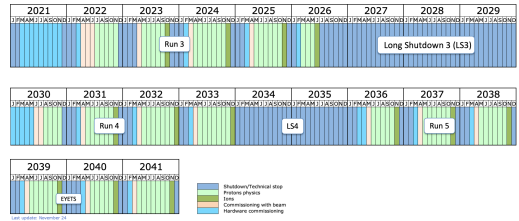
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- Upgrade to HL-LHC
- HL-LHC starts with Run 4 in 2030
- Higher instantaneous luminosity by factor 5 - 7
- Targeted integrated luminosity of 3000 fb^{-1} over 10 years of operation
- Access rare events such as $H \rightarrow \mu^+ \mu^-$
- Numerous hardware and technology upgrades
- New challenges for LHC experiments
- ATLAS upgraded in parallel

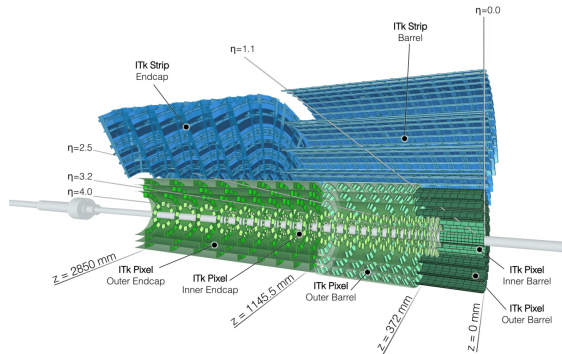


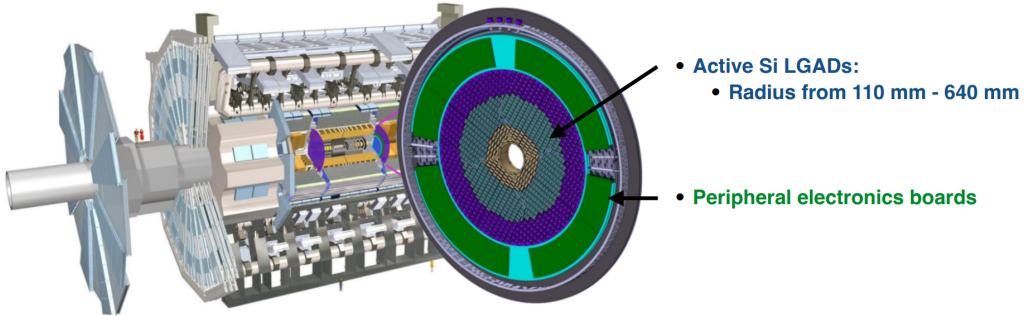
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ATLAS upgrades include but are not limited to:

- Trigger + DAQ
- Electronics Upgrades
- Full silicon ITk
- **HGTD: Silicon Timing Detector**

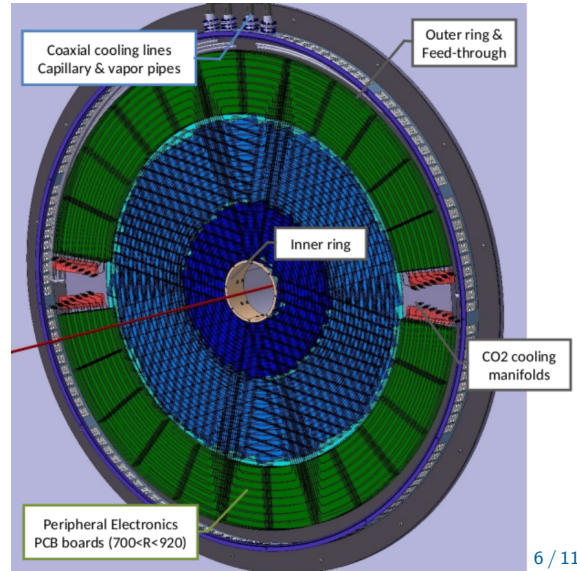




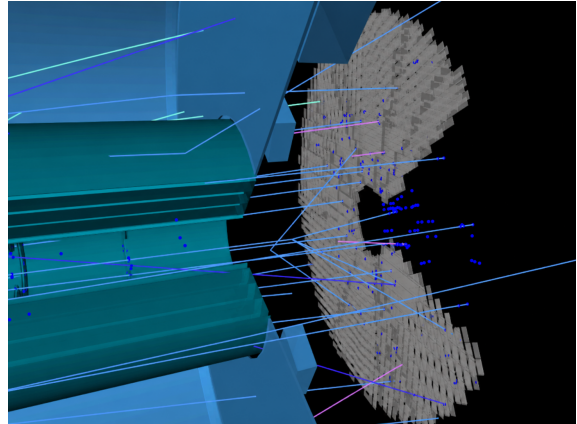
- 4D tracking hybrid Pixels
- 8032 modules
- Two instrumented double sided layers (mounted in 2 cooling disks)
- Rotated by 15°

- Detector installed on calorimeter extended barrels
- Different pixel modules designs for the different regions
- Total thickness: $< 13\text{ cm}$

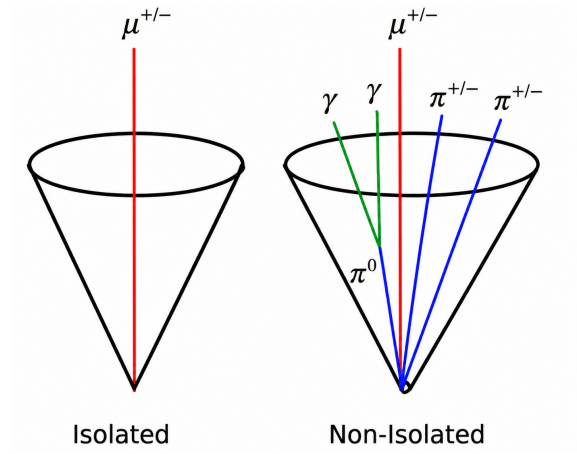
- Time measurements for objects in the forward regions of ATLAS
- $2.4 < |\eta| < 4.0$
- Active area 6.3 m^2 (total)
- Design based on $1.3 \times 1.3 \text{ mm}^2$ silicon Pixels ($2 \times 4 \text{ cm}^2$ sensors)
- Operation temperature: -30°C bi-phase CO_2 cooling
- Radiation hardness up to $5.1 \times 10^{15} n_{\text{eq}}/\text{cm}^2$ and 4.7 MGy
- Chip: ALTIROC ASIC: ATLAS LGAD Timing Integrated ReadOut Chip (CMOS)



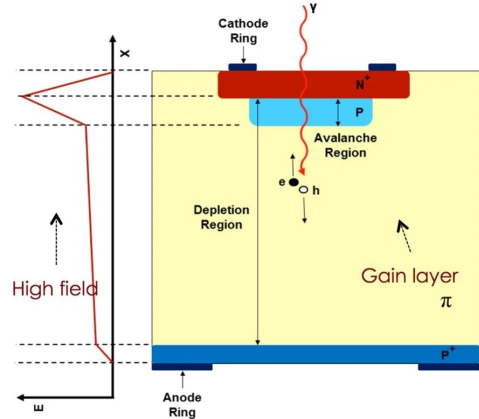
- Resolve close-by vertices
 - precise timing measurements (resolution of 30-50 ps)
- Instantaneous and unbiased luminosity measurement
- Jet pile up rejection
- Lepton isolation with time stamp



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- Silicon sensor with highly doped gain layer
- Creates strong electric field ($\sim 300 \text{ kV/cm}$)
- Controlled charge carriers avalanche multiplication
- Internal gain typically 10–30
- Increased signal-to-noise ratio
- Enables precise timing measurements with a resolution of 30–50 ps

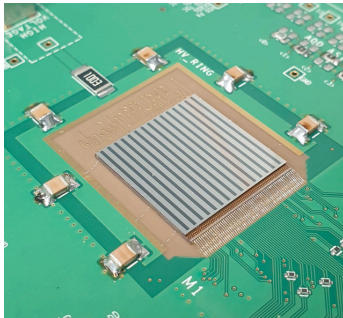


- Full HGTD integration at CERN 2027-2029
- Testing of modules and detector units during assembly
- Development of full quality-assurance procedure for surface assembly
- Final quality checks at cool
- Full system tests of the electronics and readout chain
- Commissioning of the HGTD within ATLAS and integration with the trigger and data-acquisition system during LS3



Thank you for your attention.

Backup



- Custom front-end ASIC developed for ATLAS HGTD
- 15×15 matrix of LGAD pads (225 channels)
- Measures Time-of-Arrival (ToA) and Time-over-Threshold (ToT)
- Two integrated TDCs with ~ 20 ps precision
- Low-jitter preamplifier and discriminator chain
- Power consumption < 4.5 mW per channel
- Designed for operation in the HL-LHC radiation environment
- Enables a combined timing resolution of 30–65 ps per hit with LGAD sensors

Mean energy deposition:

$$-\left\langle \frac{dE}{dx} \right\rangle = kZ^2 \frac{Z}{A} \rho \frac{1}{\beta^2} \cdot \left[\ln \left(\frac{2m_e c^2 \beta^2 \gamma^2}{I} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right) \right]$$

- $\beta = \frac{v}{c}$
- $k = 4\pi N_A r_e^2 m_e c^2 \approx 0.307 \frac{\text{MeV cm}^2}{\text{mol}}$
- $I \approx 10 \text{ eV} \cdot Z$, mean excitation energy [1].

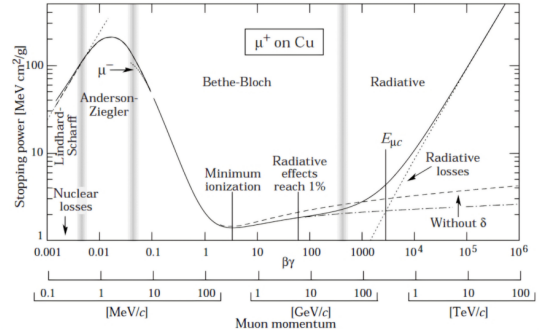


Figure: Energy deposition according to Bethe Bloch [2]

- electron ion or electron hole pairs
- electric field to separate electrons and ions or holes
- read out at charge collecting electrode
- trade-off between size $\rightarrow \frac{dE}{dx}$ more electron hole pairs and multiple scattering (low % X_0)

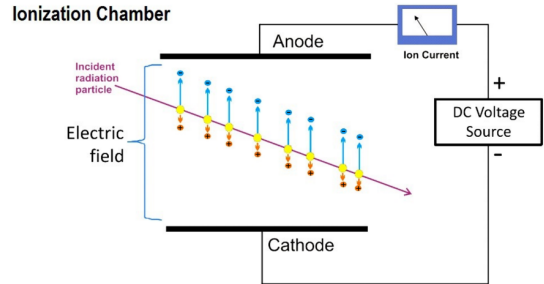


Figure: Schematic Ionisation Chamber [3]

Semiconductor

Material whose electrical conductivity lies between a conductor and an insulator. Its properties can be tuned significantly by external influences such as temperature, light and electric fields, or doping with impurities

- crystals energy levels smear to energy bands
- completely filled valence band
- empty conduction band at $T=0\text{ K}$
- small band gap
- Silicon is most important and industry standard

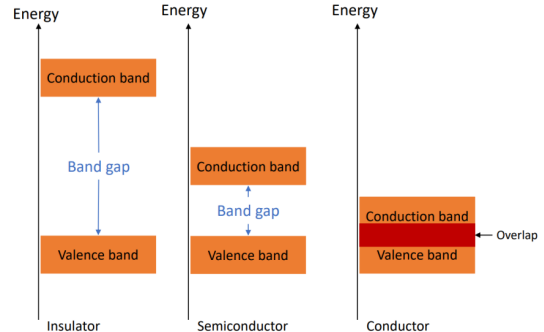


Figure: Band gap for insulator, semiconductor and conductor

Definition: Doping

Intentionally inserting impurities into a pure semiconductor crystal to alter electrical properties

- n-type (P) and p-type doping (B)
- + or - to indicate doping concentration
- Well: localised section of substrate that has been doped

Doping Example

n^- : lowly n-type doped material

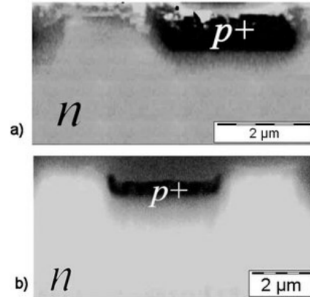


Figure: p⁺ well in n-type substrate [8]

pn junction: combine p- and n-type doped semiconductor

- diffusion
- intrinsic electric field $\rightarrow$ drift
- depletion region: free of intrinsic charge carriers
- size of depletion region depends on doping and voltage
 $\rightarrow$ lowly doped substrate for full depletion

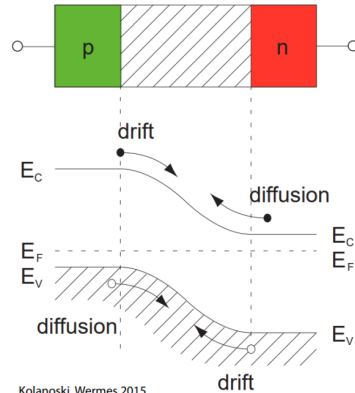


Figure: pn-junction [9]

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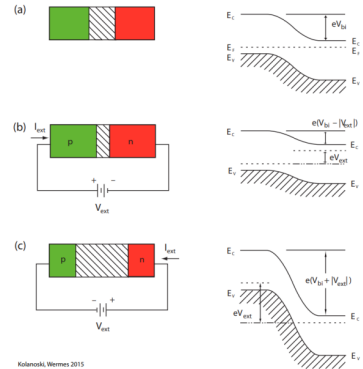


Figure: pn-junction with applied voltage [9]

pn-junction: combine p- and n-type doped semiconductor

- conduction current depends on voltage and voltage direction
- reverse bias leads to leakage current
- constant leakage current for constant temperature
- exponential dependence on the temperature [10]

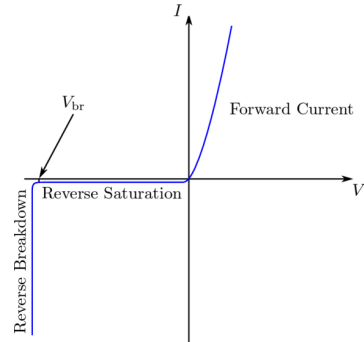


Figure: Typical I-V curve of a pn-junction [11]

- n^- doped Si
- charge collecting electrodes
- drift motion directed to electrodes at approx. const. velocity
- segmentation of the p-type doped electrode for spatial resolution
- signal = induced current $\rightarrow$ Shockley-Ramo
- challenge: separate signal and background
- diverse sources of noise, primarily thermal noise

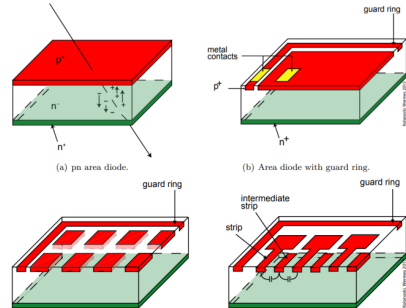
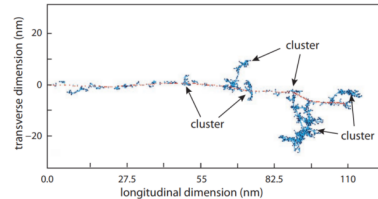
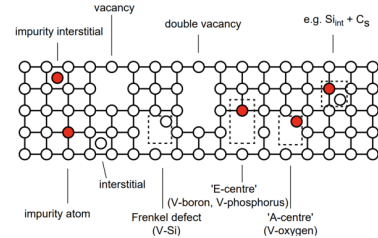


Figure: pn detector concept [9]

- exposure to high particle flux and intense radiation
- radiation damage partly reversible, partly NIEL
- collisions with the Silicon crystal lattice → vacancies and interstitials between lattice
- deep-level trap, delayed release of charge carriers → no contribution to the signal
- different particles cause a different amount of vacancies → neutron equivalent dose (neq)
- doping concentration changes → type inversion



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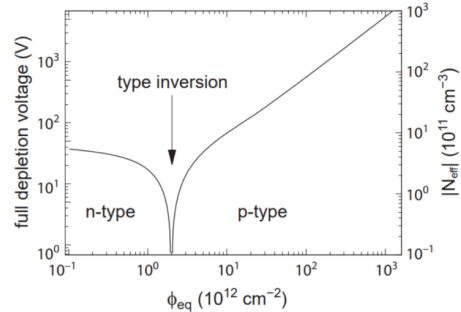


Figure: Doping concentration and type inversion[9]