

# Towards a novel silicon timing detector: ATLAS HGTD

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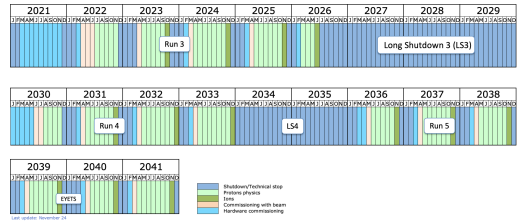
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- Upgrade to HL-LHC
- HL-LHC starts with Run 4 in 2030
- Higher instantaneous luminosity by factor 5 - 7
- Targeted integrated luminosity of  $3000 \text{ fb}^{-1}$  over 10 years of operation
- Access rare events such as  $H \rightarrow \mu^+ \mu^-$
- Numerous hardware and technology upgrades
- New challenges for LHC experiments
- ATLAS upgraded in parallel

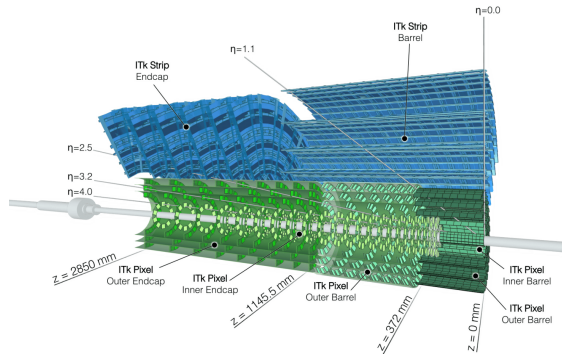


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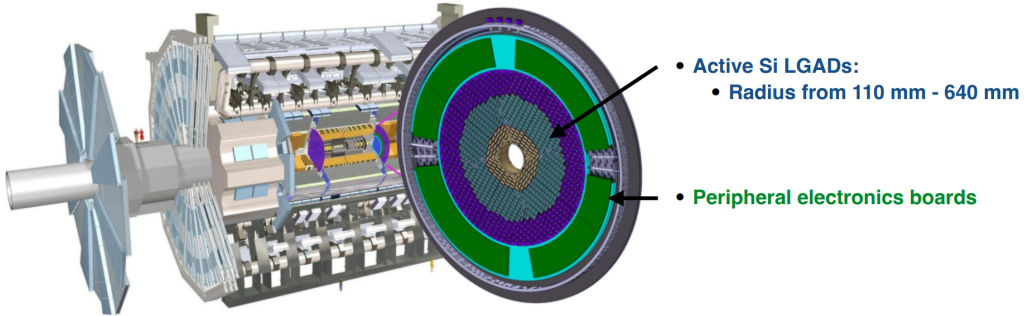


ATLAS upgrades include but are not limited to:

- Trigger + DAQ
- Electronics Upgrades
- Full silicon ITk
- **HGTD: Silicon Timing Detector**



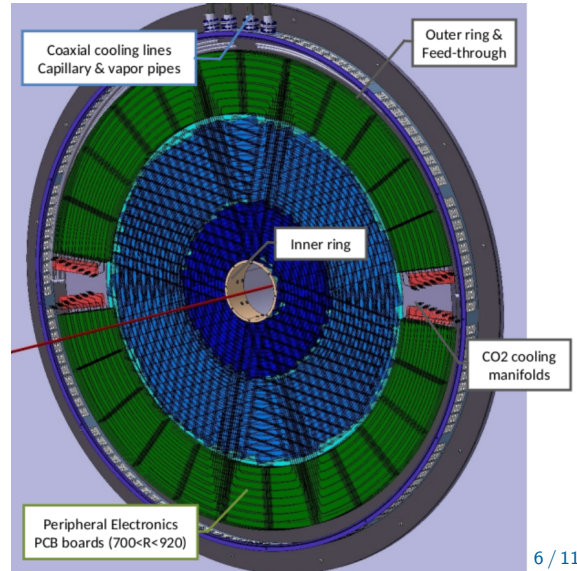




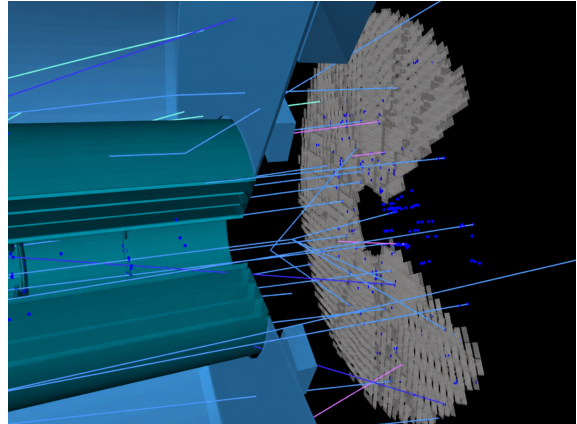
- 4D tracking hybrid Pixels
- 8032 modules
- Two instrumented double sided layers (mounted in 2 cooling disks)
- Rotated by  $15^\circ$

- Detector installed on calorimeter extended barrels
- Different pixel modules designs for the different regions
- Total thickness:  $< 13$  cm

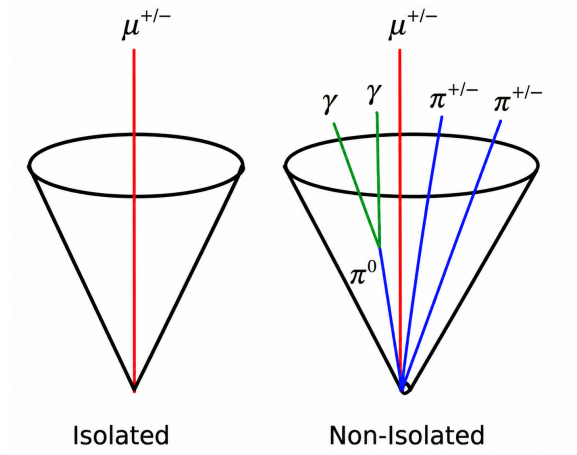
- Time measurements for objects in the forward regions of ATLAS
- $2.4 < |\eta| < 4.0$
- Active area  $6.3 \text{ m}^2$  (total)
- Design based on  $1.3 \times 1.3 \text{ mm}^2$  silicon Pixels ( $2 \times 4 \text{ cm}^2$  sensors)
- Operation temperature:  $-30^\circ\text{C}$  bi-phase  $\text{CO}_2$  cooling
- Radiation hardness up to  $5.1 \times 10^{15} n_{\text{eq}}/\text{cm}^2$  and  $4.7 \text{ MGy}$
- Chip: ALTIROC ASIC: ATLAS LGAD Timing Integrated ReadOut Chip (CMOS)



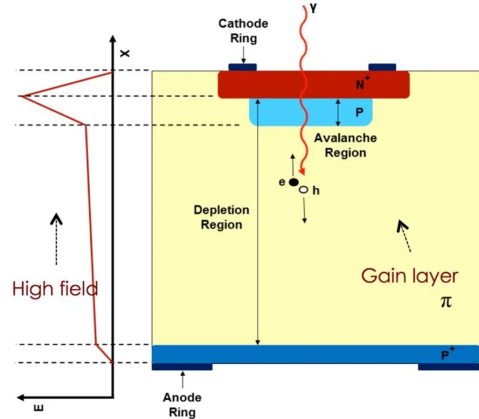
- Resolve close-by vertices
  - precise timing measurements (resolution of 30-50 ps)
- Instantaneous and unbiased luminosity measurement
- Jet pile up rejection
- Lepton isolation with time stamp



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- Silicon sensor with highly doped gain layer
- Creates strong electric field ( $\sim 300 \text{ kV/cm}$ )
- Controlled charge carriers avalanche multiplication
- Internal gain typically 10–30
- Increased signal-to-noise ratio
- Enables precise timing measurements with a resolution of 30–50 ps



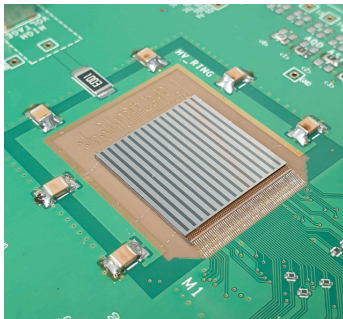
- Full HGTD integration at CERN 2027-2029
- Testing of modules and detector units during assembly
- Development of full quality-assurance procedure for surface assembly
- Final quality checks at cool
- Full system tests of the electronics and readout chain
- Commissioning of the HGTD within ATLAS and integration with the trigger and data-acquisition system during LS3



**Thank you for your attention.**

# Backup





- Custom front-end ASIC developed for ATLAS HGTD
- $15 \times 15$  matrix of LGAD pads (225 channels)
- Measures Time-of-Arrival (ToA) and Time-over-Threshold (ToT)
- Two integrated TDCs with  $\sim 20$  ps precision
- Low-jitter preamplifier and discriminator chain
- Power consumption  $< 4.5$  mW per channel
- Designed for operation in the HL-LHC radiation environment
- Enables a combined timing resolution of 30–65 ps per hit with LGAD sensors