Hardware Upgrade of the ATLAS LAr Purity System for the High Luminosity LHC

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The primary objective of this research is the complete redesign of an existing Front End Board for the Liquid Argon Purity System, developed as part of the Phase II Upgrade of the ATLAS experiment at CERN. This upgrade will take place during the second long shutdown, beginning next year and extending over a period of three years, in preparation for the High Luminosity LHC. A central motivation for the redesign arises from the unavoidable requirement of a negative voltage supply, which is currently provided externally but will no longer be available in the upgraded configuration. To address this, the new Front End Board for the Purity System must incorporate an integrated voltage converter capable of generating the necessary supply internally. A schematic of the new power solution is shown in figure 1.
Taking this necessity as an opportunity, the board is not only being adapted but comprehensively redesigned from the ground up. The updated design implements improved impedance control, enhanced routing enabled by the addition of two extra layers, and the introduction of additional ground and power planes. These measures collectively contribute to better signal integrity, reduced noise susceptibility, and a more robust distribution of power across the board. As a result, the new Front End Board design improves performance, ensuring stability and reliability in the demanding environment of the HL-LHC.

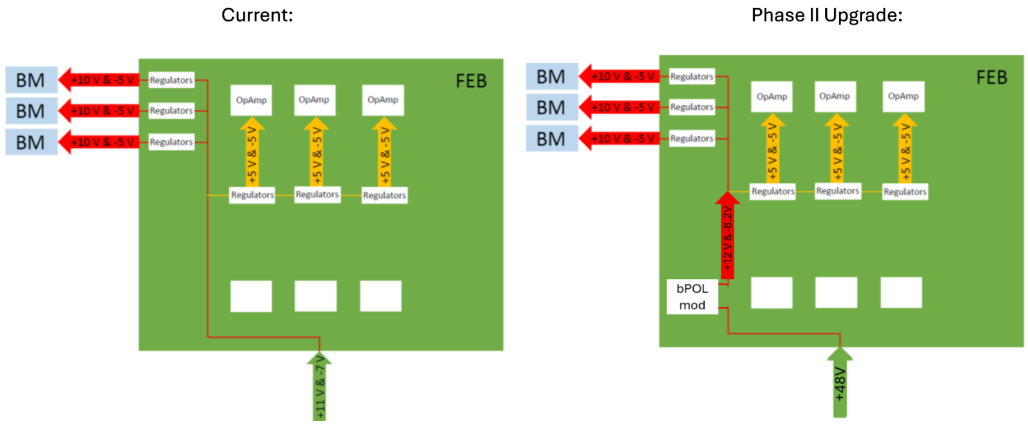

Abbildung 1: Schematic of the Front End Board (FEB) for both the current version (left) and the planned Phase II Upgrade (right). The main focus is on the power distribution of the board.

The presentation begins with a brief overview of the motivation for the Purity system, outlining its purpose and importance within the ATLAS experiment. This is followed by an introduction to the current implementation of the Purity system, with particular emphasis on the underlying requirement for a negative voltage supply. The presentation explains why this approach is necessary in contrast to the alternative of relying on a floating ground and maintaining operation with only positive voltages, as will be the case for most other subsystems in the future.
Subsequently, the schematic of the existing Front End Board is presented and discussed, providing insight into its current design and limitations. This serves as a basis for a comparison between the voltage currently supplied to the system and the voltage that will be available in the future, highlighting the emerging challenge. A schematic solution to this issue, based on the integration of a voltage converter, is then introduced.
Finally, both the current and the newly developed Front End Board designs are presented successively. This comparison serves to illustrate the improvements and optimizations that have been achieved and demonstrating the progress made towards a robust and design for the Purity system within the HL-LHC environment.