All Silicon Modules

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In high energy physics, detector systems are an essential part of the measuring apparatus for discovering new and exciting phenomena. One important part of many detectors is the tracking system, usually built from semiconductor and/or gas detectors with special attention to silicon pixel detectors, as they achieve high spatial and time resolution, while remaining fairly affordable and having low material budget.

Silicon pixel detectors can be manufactured in a standard CMOS process and come in different form factors (e.g. monolithic vs hybrid). The chip size is limited by the foundaries reticle size of typically $20 - 25\,\mathrm{mm}$. As large areas need to be covered, many chips are needed and combined to larger modules. Although there is a method called stitching, which makes it possible to create chips larger than the reticle size limit, however, this technic reduces yield and is not cost effective for HEP.

Instead in a waver probing step, each chip is tested before dicing and working chips are then combined into Modules. Modules include chips (and sensors), PCBs, SMD components, and connectors to mechanically and electrically connect all parts together to create larger sizes.

As one can imagine, the material budget for silicon pixel detectors is not much, but can be substantial if all PCB layers, SMD components, cooling and mounting hardware, etc. are considered. Also the work required to build modules is fairly high with many manufacturing steps and usually several companies involved.

To minimize material budget and manufacturing complexity, the number of components must be reduced. To achieve this, the topic of this PhD thesis is to build *All Silicon Modules*.

The concept assumes to find four working chips in a row in the wafer probing step and cut them as one large part instead of dicing the wafer in each chip individually. After cutting the module, metal and isolation layers create electrical paths between chips and lead to wire bonding pads on one end of the module.

The challenges with this approach reach from structural considerations over thermal and cooling options to the electrical paths on the module.

This thesis works closely together with the Belle Collaboration where *All Silicon Modules* based on Obelix chips are planned to be installed in the next upgrade phase of the inner vertex detector (iVTX) starting 2028. It will also look at the capabilities of this approach in a more general sense with different chips/chip types and requirements in different detector systems. .