Developments in the ITk OB Demonstrator DCS

Anne Gaa

Universität Göttingen

The Detector Control System (DCS) of the ITk pixel detector monitors the detector environment, provides a failsafe in form of the interlock system, and handles power and control of the hardware as well as communication between subsystems. The DCS consists of power supplies, sensors, and services, as well as the interlock system, and the software. The Supervisory Control and Data Acquisition (SCADA) system of the DCS is a distributed system of WinCC OA using the JCOP framework.

One part of its readout is the Monitoring of Pixel System (MOPS), which provides temperature and voltage monitoring of the front-end modules as well as the optoboxes. In the MOPS readout chain, the MOPShub is the bidirectional interface between the local DCS station and the MOPS chips. Data is aggregated from the MOPS chips and sent to the DCS control station, while the DCS station sends control commands the other way. The ITk DCS will manage the readout of about 1200 MOPS chips inside the final detector.

The final version of the MOPS readout chain is not available yet for use in the testing sites, because both the Embedded Monitoring and Control Interface (EMCI) as well as the Embedded Monitoring Processor (EMP) are not available. Additionally, the capacity needed to have a full readout with EMCI and EMP in all testing sites would exceed the amount of hardware needed in the final detector. Therefore, the MOPShub for Beginners (MhfB) was created.

MhfB is a simplified version of the MOPS readout chain. Its hardware components are the backplane where up to four CICs can be inserted, as well as a RaspberryPi (RPi), which takes over the functionality of the EMCI and EMP. This means that it codes and decodes the CAN messages sent to the MOPS chips, as well as hosts an OPC UA client which sends the data to an OPC UA server. On WinCC OA, another OPC UA client connects to the same OPC UA server, and the data is transferred to the local DCS station.

Due to an increasing readout capacity needed for the testing sites, a new intermediary readout chain is needed. The current plan for this intermediary readout chain can be seen in Fig. 1. Here, a Xilinx FPGA fulfills the funcionality of the EMCI and EMP. Aside from an increased capacity, there is also new hardware incorporated in the form of the PP3-FPGA.

My work on this readout chain will include developing the OPC UA server located on the FPGA that will replace the EMCI and EMP. For this, the client and subscriber model of the MhfB project will need to be rewritten, with the new OPC UA server having access to the common register of the FPGA.

For similar use cases of OPC UA servers, a register simulator was created by the ATLAS Central DCS team. This simulator provides a development environment for these OPC
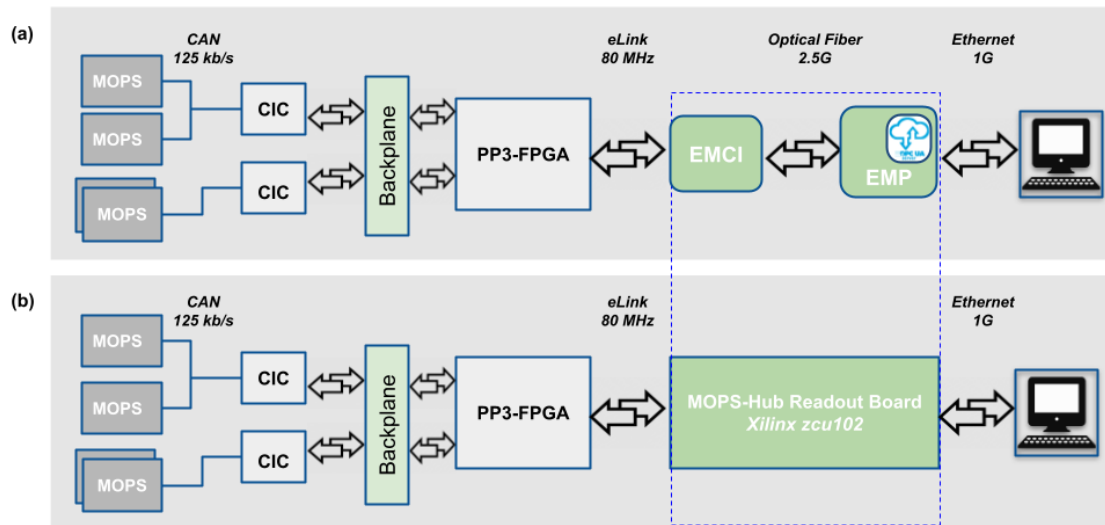
Abbildung 1: Schematics of the intermediary MOPS readout chain.

UA servers based on the register mapping of the use case. This allows the development of the OPC UA server without the necessity of the hardware and its setup. A register simulator for the OPC UA server of the MOPS readout chain also gives future users of the OPC UA server the opportunity to test changes in an environment without the hardware, making these tests easier.

The timeline for the new MOPS readout chain with increased capacity is to have a first iteration done at the end of the year, so that the roll-out to the testing sites can be performed, starting next year.